Overview of Risk Mitigation Testing – Electrical

ERAI Conference - April 18 & 19, 2013

Clifton Aldridge

Laboratory Manager

Dynamic Research and Testing Laboratories, LLC

Dynamic Research and Testing Laboratories, LLC is located in Albuquerque New Mexico. The Laboratory is within the Electronic Contract Manufacturer "IEC Electronics"

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

DRTL Organizational Chart

Mark Northrup
(Director of Laboratory)

Clifton Aldridge
(Laboratory Manager)

Jodi Wahl
(Marketing Coordinator)

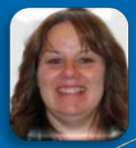
Holly Connelly
(Administrative Specialist)

Teri Kovaleski
(Human Resources)

Chris Hoover
(Quality Assurance)

Christine Glomski
(Internal Auditor)

Karin Zimmerer
(Document Control)



DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

DRTL Organizational Chart

Mark Northrup
(Director of Laboratory)

Clifton Aldridge
(Laboratory Manager)

Rachel Garcia
(Device Analyst II)

James Taylor
(Failure Analysis Engineer)

Tony James
(Failure Analysis Engineer)

JR Lucero
(Device Technician)

Robert Perea
(Device Technician)

Nabahe “Bo” Tewawina
(Device Technician)

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Dynamic Research and Testing Laboratories, LLC

Navigating the Electrical Test Requirements When Procuring from Non-OCMs

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Electrical Test

Current Specifications

- AS5553 Fraudulent/Counterfeit Electronic Parts; Avoidance, Detection, Mitigation, and Disposition

- AS6081 Fraudulent/Counterfeit Electronic Parts; Avoidance, Detection, Mitigation, and Disposition – Distributors

- AS6171 (Not Released) Test Methods Standard; General Requirements, Suspect/Counterfeit Electrical, Electronic, and Electromechanical Parts

- CCAP-101 Counterfeit Components Avoidance Program Certification

- TB-0003 Counterfeit Parts & Materials Risk Mitigation

- GIFAS 5052 208 Guide for managing electronic component sourcing through non-franchised distributors. Preventing fraud and counterfeiting.

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Electrical Test

- **AS5553 Fraudulent & Counterfeit Electronic Parts**
- **Avoidance, Detection, Mitigation, and Disposition**

E.1.10 Electrical Testing

Comprehensive electrical testing should be performed on all parts, across the full temperature range as per the parts' specification, in facilities with test equipment and test engineering expertise suitable for the specific part type. The acquiring activity should approve all test facilities and test methodologies. This test may be life limiting.

E.1.11 Burn-In

Pre Burn-In and Post Burn-In electrical testing should be performed on all parts using the criteria as defined in the applicable part specification. The steps involved in performing burn-in test are described below. This test may be life limiting.

a. Pre Burn-In Electrical Performance Testing - Parts should undergo comprehensive electrical testing to the applicable performance data sheet.

b. Burn-In - Parts (100%) should undergo a powered burn-in at the component's/part's maximum rated temperature.

c. Post Burn-In Electrical Performance Testing - Parts should undergo comprehensive electrical testing to the applicable performance data sheet.

Electrical Test

- **AS6081 Fraudulent & Counterfeit Electronic Parts**
- **Avoidance, Detection, Mitigation, and Disposition - Distributors**

C.3 ELECTRICAL TESTING

Comprehensive electrical testing should be performed on all parts in a facility with test equipment and test engineering expertise suitable for the specific part type. The Customer should approve all test facilities and test methodologies.

C.4 BURN-IN

Pre Burn-In and Post Burn-In electrical testing should be performed on all parts. The steps involved in performing burn-in test are described below.

a. Pre Burn-In Electrical Performance Testing - Parts should undergo comprehensive electrical testing to the applicable performance data sheet.

b. Burn-In - Parts (100%) should undergo a powered burn-in at the part's maximum rated temperature.

c. Post Burn-In Electrical Performance Testing - Parts should undergo comprehensive electrical testing to the applicable performance data sheet.

Electrical Test

AS6171 (Not Released) Test Methods Standard; General Requirements, Suspect/Counterfeit Electrical, Electronic, and Electromechanical Parts

- AS6171 provides further detail to the electrical test requirements
  - 3.4.1.6 Electrical –AS6171Test Method VI
  - Such electrical testing shall be performed using appropriate requirements as specified in related SMDs, MIL-PRFs, manufacturer datasheets or customer supplied requirement documents.
  - Sampling plan calls for 116devices/c=0 tested with no failures allowed. This gives a 90 percent confidence that the percentage failures is at most 2%.
  - The type and extent of electrical testing is so complex to try to screen-out counterfeit parts that it is the responsibility of the User Engineer to make the determination of the specific test requirements that shall be documented in a Test Requirements document that shall become part of a Statement of Work (SOW).
  - The minimum level of electrical testing for the Low Risk Level is defined as the DC Test for Active Devices and Value Measurement for Passive Devices. At the minimum level the tests shall be performed at ambient temperature
  - Detailed guidance provided in AS6171 TEST METHOD VI

Electrical Test

AS6171 (Not Released) Test Methods Standard; General Requirements, Suspect/Counterfeit Electrical, Electronic, and Electromechanical Parts

TABLE C-1 EXAMPLES OF ACTIVE DEVICES KEY ELECTRICAL PARAMETERS

PART CATEGORY	TYPE	KEY ELECTRICAL PARAMETERS	MIL STD/SPEC
Microcircuit - Linear	(Generic LM111	Input offset voltage & current, raised input offset voltage & current, input bias, collector output voltage (strobed), common mode rejection, low level output voltage, input & output leakage current, pos. & neg. supply current, temp. coeff. Of input offset V & I , Output short circuit current, adj. for input offset volt., volt. Gain, response time(collector output)	DLA SMD 5962-00524
	Operational Amplifiers, Quad, Precision (Generic OP484)	Input offset voltage; Average input offset voltage; Input offset current; Input bias current; Common mode rejection ratio; Power supply rejection ratio; Output high voltage; Output low voltage; Large signal voltage gain; Supply current; Slew rate	DLA SMD 5962-00517
	(Generic AD904)	Vcc supply current; Power dissipation; Power supply rejection ratio; Offset error; Gain error; Input voltage range; Input logic high & low voltage; Input logic high & low current; Output logic high & low voltage; Differential non-linearity; Signal to noise ratio; Signal to noise and distortion ratio; Worst spur ratio	DLA SMD 5962-02538
Microcircuit - Digital	Octal Bus Transceiver and Register (Generic 54BCT646)	High & low level output voltage; Input clamp voltage; High & low level input current; Short-circuit output current, Supply currents; Functional tests to verify the Truth table of the SMD; Max. clock frequency; Propagation delay times	DLA SMD 5962-91555
Microcircuit - Memory	SRAM (Static Random Access Memory), 2M x 8 Bit	Output high & low voltage; Input and output leakage current; Supply currents, Data retention current; Propagation delay times (Address/Chip Enable/Output Enable to data valid, including the write cycle set-up parameters); Functional tests to verify proper operation of SRAM as specified in Appendix A of the SMD (Check all memory cells by using the following algorithms: Checkerboard/checkerboard-bar, March, XY March CE deselect checkerboard/ checkerboard-bar or	DLA SMD 5962-08219

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Electrical Test

CCAP-101 COUNTERFEIT COMPONENTS AVOIDANCE PROGRAM, CERTIFICATION

4.9.6 Passive components

All unmarked passive components (both Level A & B) or not contained in OCM original and verified packaging shall be sample tested, 30 pcs/1000 components for parameters specified below.
The tests shall be in accordance with OCM data sheets or military specifications as applicable.

A. Capacitors:
- Capacitance and tolerance at 25 ^{0}C and min/max temp
- DWV
- Dissipation factor as applicable
- ESR (Electrolytics only)

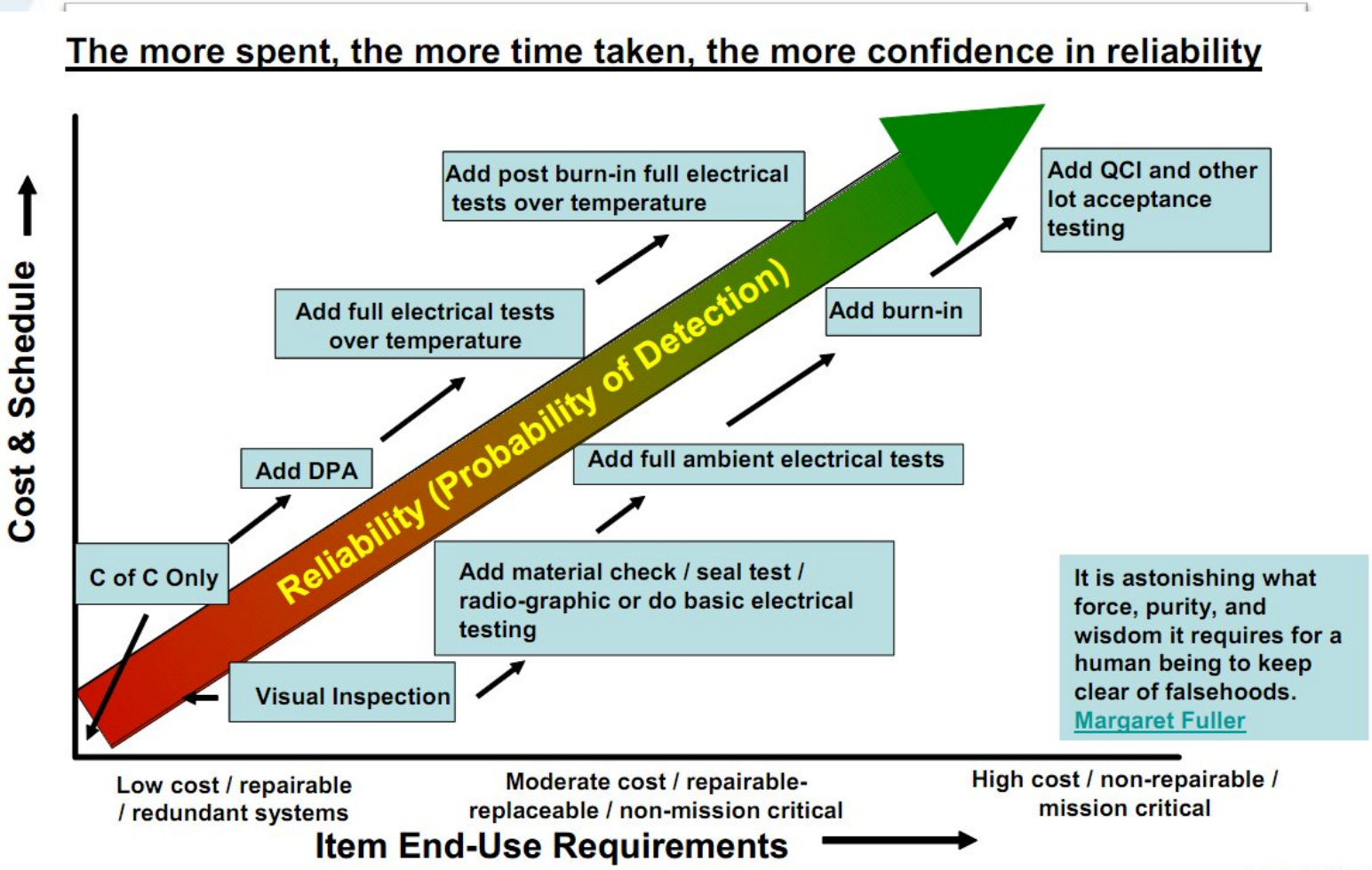
B. Inductors:
- Inductance over or within specified frequency and temperature range
- Q
- Series resistance

C. Resistors:
- Resistance and tolerance at 25 ^{0}C and min/max temp.
- Temperature coefficient

D. Other Passives
- Applicable parameters

Electrical Test

TB-0003 Counterfeit Parts & Materials Risk Mitigation



TB-0003

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC

DRTL

A Member of the IEC Electronics Family of Companies

Electrical Test

GIFAS 5052 208 Guide for managing electronic component sourcing through non-franchised distributors. Preventing fraud and counterfeiting

E. Electrical tests

This is a test conducted at room temperature on a per unit or sampling basis, depending on the inspection lot and/or package size, in order to verify the electrical characteristics specified by the manufacturer. This test may be accompanied by tests at operating temperature and life testing, depending on the level of quality required and the criticality of the application.

All electrical and physical tests and analyses must be performed by an internal or outside specialist and recognized laboratory.

GIFAS/5052/2008

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

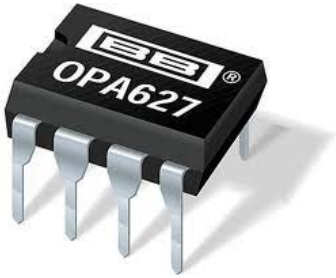
Electrical Test

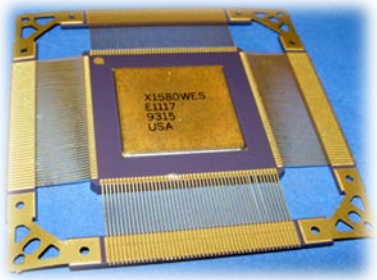
When did "Requirement Specifications" become "Guidance Documents" leaving interpretation to the operator, tester, or user (e.g., Technician, Component Engineer, Program Manager, etc.) ?

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Electrical Test

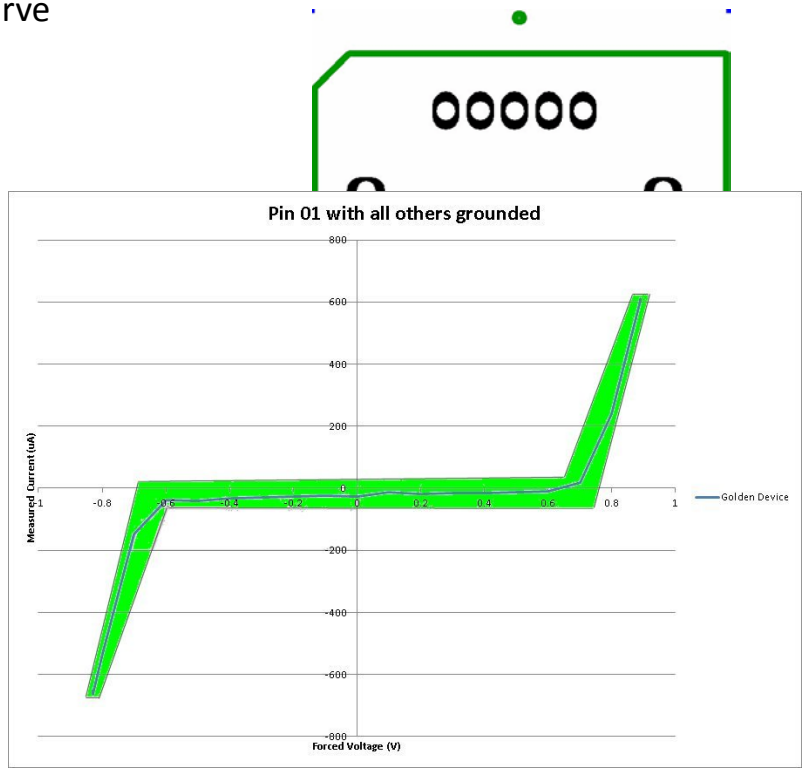
- Basic building block devices may be more attractive for counterfeiting
  - Examples : Op-amps, comparators, low level logic, ADCs, DACs, MOSFETs, Diodes, Capacitors, Resistors…
  - Pros for the counterfeiter
    - Larger selection of pin for pin capable devices to substitute
    - Typical designs may have large margins allowing of passage of system level checks
  - Cons for the counterfeiter
    - Typically lower cost devices
    - May need large volume for same price point
- Complex devices (FPGAs, CPU, SIC…)
  - Xilinx, Motorola, and Intel ?
  - Have system security features in the chip (e.g., embedded at the die level) to difficult to repeat or defeat?
  - Most likely will not pass the board assembly system level electrical verification/functional testing?

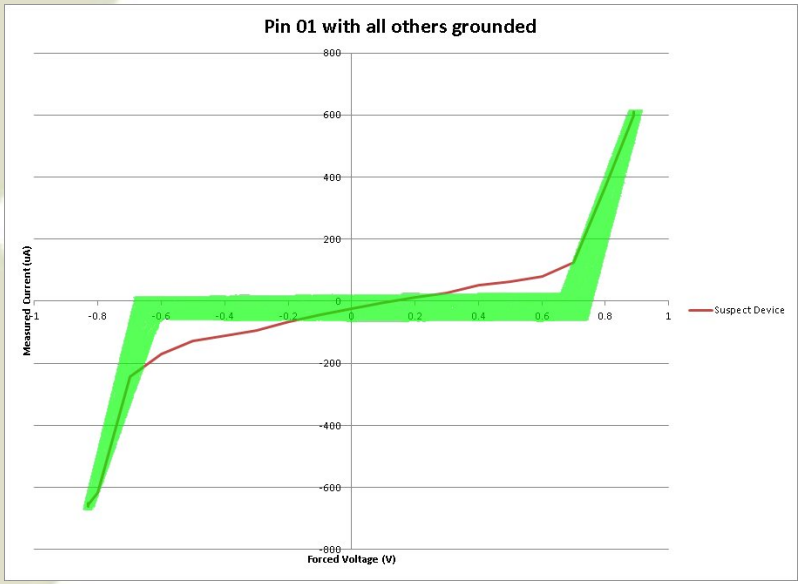




Going Beyond Simple Pin to Pin Testing

- Obtain Current vs Voltage (IV) curve for golden device
- Software defines passing limits around the golden device curve
- Software builds a mask around the golden device curve
- Suspect devices IV curves obtained
- Suspect devices tested in comparison to the golden device
- Suspect devices tested even with slight damage can be detected.

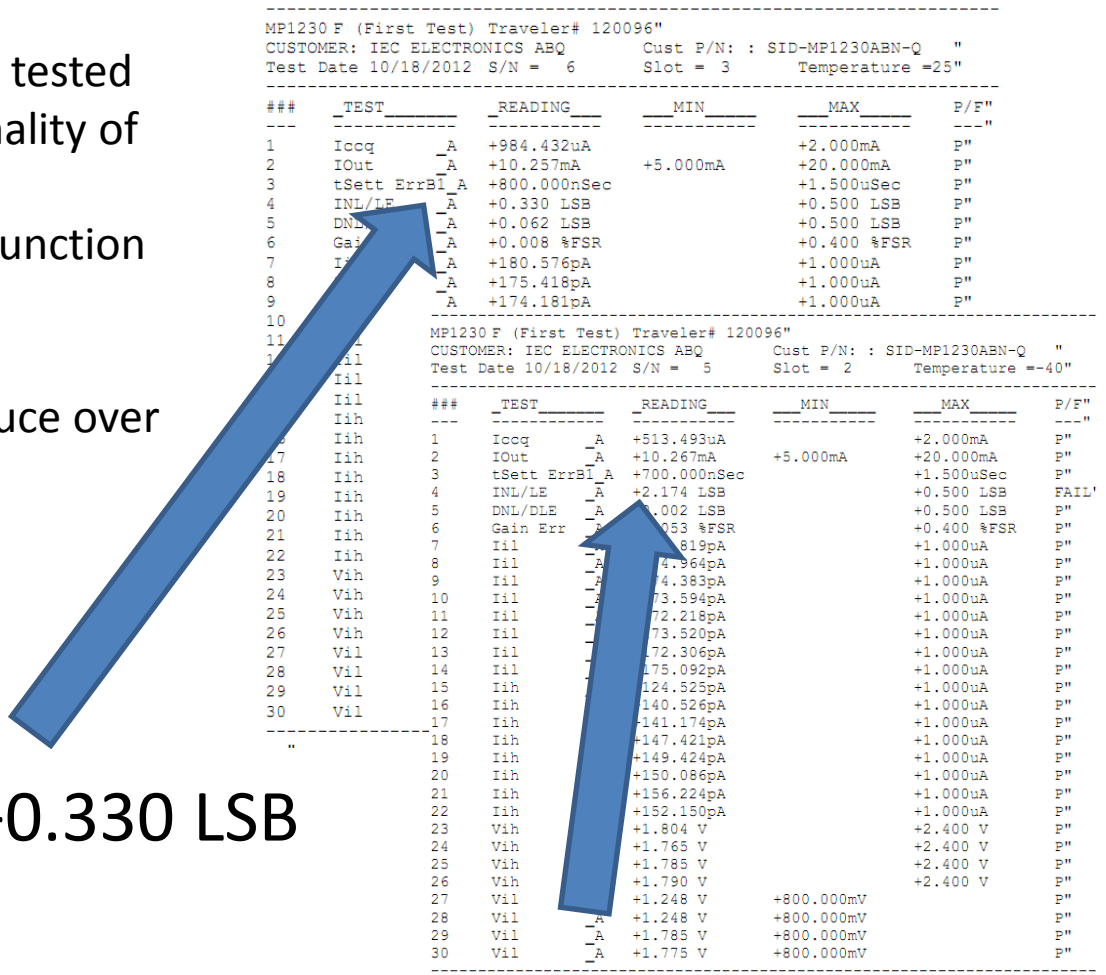




DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Full Functional Testing

- Key Parameters may need to be tested in order to validate the functionality of the device under test.
- Devices having the same basic function may not have the same over all performance.
- Degraded performance can reduce over all design margins and system performance.



MP1230 F (First Test) Traveler# 120096"
CUSTOMER: IEC ELECTRONICS ABQ Cust P/N: : SID-MP1230ABN-Q "
Test Date 10/18/2012 S/N = 6 Slot = 3 Temperature =25"

###	_TEST_____	_READING___	___MIN_____	___MAX_____	P/F"
1	Iccq _A	+984.432uA		+2.000mA	P"
2	IOut _A	+10.257mA	+5.000mA	+20.000mA	P"
3	tSett ErrBl_A	+800.000nSec		+1.500uSec	P"
4	INL/LE _A	+0.330 LSB		+0.500 LSB	P"
5	DNL _A	+0.062 LSB		+0.500 LSB	P"
6	Gai _A	+0.008 %FSR		+0.400 %FSR	P"
7	I _A	+180.576pA		+1.000uA	P"
8	_A	+175.418pA		+1.000uA	P"
9	_A	+174.181pA		+1.000uA	P"
10					
11	Iil				
12	Iil				
13	Iil				
14	Iih				
15	Iih				
16	Iih				
17	Iih				
18	Iih				
19	Iih				
20	Iih				
21	Iih				
22	Iih				
23	Vih				
24	Vih				
25	Vih				
26	Vih				
27	Vil				
28	Vil				
29	Vil				
30	Vil				

"

MP1230 F (First Test) Traveler# 120096"
CUSTOMER: IEC ELECTRONICS ABQ Cust P/N: : SID-MP1230ABN-Q "
Test Date 10/18/2012 S/N = 5 Slot = 2 Temperature =-40"

###	_TEST_____	_READING___	___MIN_____	___MAX_____	P/F"
1	Iccq _A	+513.493uA		+2.000mA	P"
2	IOut _A	+10.267mA	+5.000mA	+20.000mA	P"
3	tSett ErrBl_A	+700.000nSec		+1.500uSec	P"
4	INL/LE _A	+2.174 LSB		+0.500 LSB	FAIL'
5	DNL/DLE _A	.002 LSB		+0.500 LSB	P"
6	Gain Err _A	053 %FSR		+0.400 %FSR	P"
7	Iil _A	819pA		+1.000uA	P"
8	Iil _A	4.964pA		+1.000uA	P"
9	Iil _A	4.383pA		+1.000uA	P"
10	Iil _A	73.594pA		+1.000uA	P"
11	Iil _A	72.218pA		+1.000uA	P"
12	Iil _A	73.520pA		+1.000uA	P"
13	Iil _A	72.306pA		+1.000uA	P"
14	Iil _A	175.092pA		+1.000uA	P"
15	Iih _A	124.525pA		+1.000uA	P"
16	Iih _A	140.526pA		+1.000uA	P"
17	Iih _A	141.174pA		+1.000uA	P"
18	Iih _A	+147.421pA		+1.000uA	P"
19	Iih _A	+149.424pA		+1.000uA	P"
20	Iih _A	+150.086pA		+1.000uA	P"
21	Iih _A	+156.224pA		+1.000uA	P"
22	Iih _A	+152.150pA		+1.000uA	P"
23	Vih _A	+1.804 V		+2.400 V	P"
24	Vih _A	+1.765 V		+2.400 V	P"
25	Vih _A	+1.785 V		+2.400 V	P"
26	Vih _A	+1.790 V		+2.400 V	P"
27	Vil _A	+1.248 V	+800.000mV		P"
28	Vil _A	+1.248 V	+800.000mV		P"
29	Vil _A	+1.785 V	+800.000mV		P"
30	Vil _A	+1.775 V	+800.000mV		P"

Integral Non-Linearity +0.330 LSB

Integral Non-Linearity +2.174 LSB

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

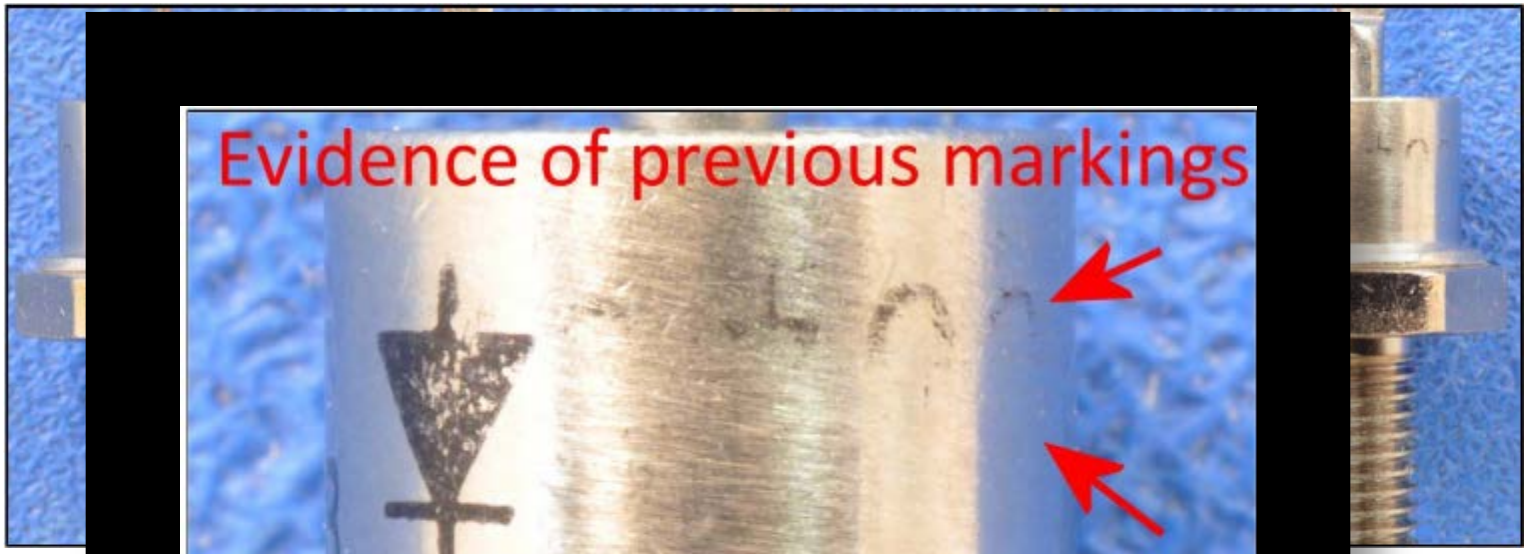
Full Functional Testing

			Q7 (IRF540S)				Q8 (IRFR024)			
			Suspect	Exemplar	Limits		Suspect	Exemplar	Limits	
Test		Units	SN 2148	SN 1088	Min	Max	SN 2148	SN 1088	Min	Max
BVDSS	Initial	V	114.4	113.6	100		64.1	67.6	55	
rdsON (17A and 10A respectively)		ohms	0.047	0.051		0.077	0.053	0.066		0.075
Vgsth		V	2.57	2.74	2	4	1.66	2.78	2	4

			Q7 (IRF540S)				Q8 (IRFR024)			
			Suspect	Suspect	Limits		Suspect	Suspect	Limits	
Test		Units	SN 6150	SN 0151	Min	Max	SN 6150	SN 0151	Min	Max
BVDSS	Initial	V	121.1	106.3	100		64.1	64.6	55	
rdsON (17A and 10A respectively)		ohms	0.05	0.055		0.077	0.074	0.078		0.075
Vgsth		V	2.57	2.78	2	4	3.33	3.02	2	4
BVDSS	Post HAST	V	121.3	106.2	100		64.1	64.7	55	
rdsON (17A and 10A respectively)		ohms	0.051	0.055		0.077	0.073	0.077		0.075
Vgsth		V	2.57	2.78	2	4	3.32	3.02	2	4
BVDSS	Post Thermal Shock	V	121	106.2	100		64.2	64.7	55	
rdsON (17A and 10A respectively)		ohms	0.051	0.054		0.077	0.074	0.078		0.075
Vgsth		V	2.57	2.77	2	4	3.33	3.02	2	4

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Electrical Test



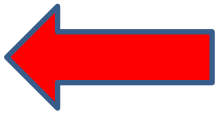
DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC

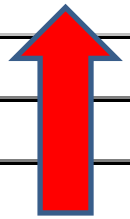
DRTL

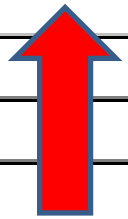
A Member of the IEC Electronics Family of Companies

Electrical Test

S/N	V_Z 7.125 – 7.875 V I_R = 335 mA	I_R 100 uA max. V_R = 5.7 V	V_Z for a 1N3000RB 58.9 – 65.1 V I_R = 40 mA	I_R for a 1N3000RB 10uA max. V_R = 47.1 V
1	<1000V	0.011 uA		
2	59V @ 40 mA	144.6 uA	59V	1710 uA







Comments: SN 1 appears to be a switching power diode with a reverse breakdown of ~1200V. No signs of leakage or damage of the diode detected. SN 2 appears to be a 62V Zener diode. This diode appears to be a 1N3000RB, however would still fail the reverse current measurement for this device type as well.

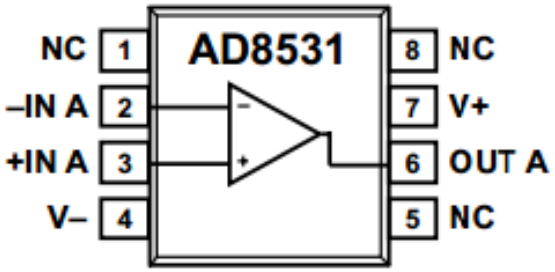
DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC

DRTL

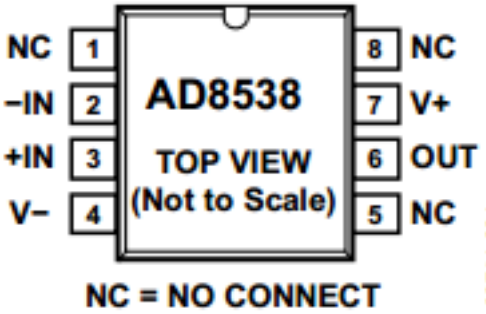
A Member of the IEC Electronics Family of Companies

Electrical Test

Input Offset, Vos 25mV max
Output Current 250mA
Supply Current, Icc 1 mA



Input Offset, Vos 13uV max
Output Current 25mA
Supply Current, Icc 180 uA

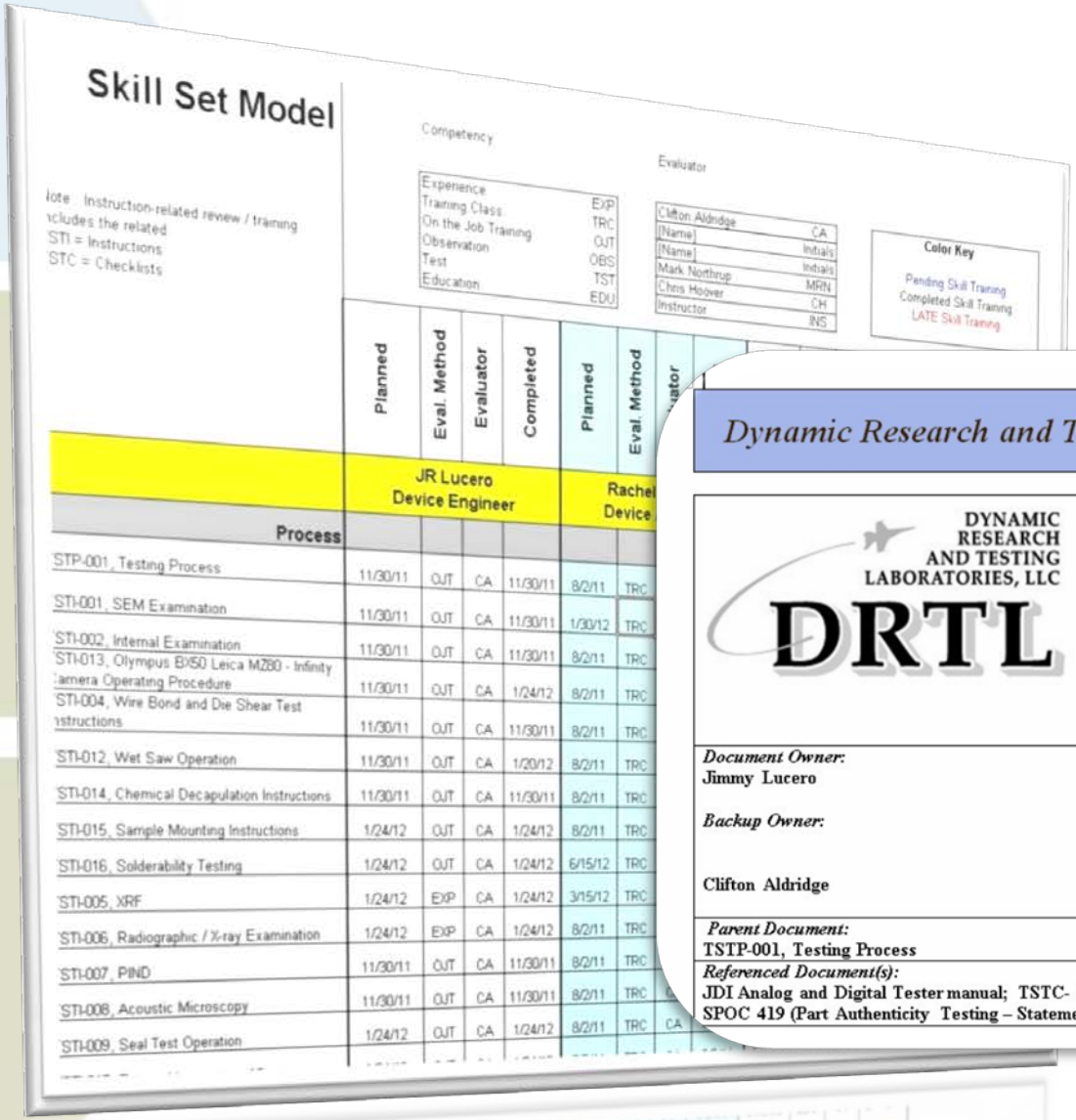


DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Summary of Electrical Test Issues

- **Current risk mitigation standards are open to interpretation which breeds inconsistency across test facilities in actual test performed and costs.**
- Paramount to understand end use (Avionics, Missile, Industrial, Medical)
- Completely define test requirements (DCs, Acs Functional, Over Temp).
- Best case is to have the user define important parameters to tested based on the functionality of the device or based on the requirements of the design
- The user may not have access to design information, however the test facility sould provide different options or levels based on the functionality of the device.
- Suggest read and record data be required for all parameters (data can be reviewed not just failing parameters). Industry Database?
- Recommendations?

ISO 17025 Skill Set Model



Skill Set Model

Competency

Experience	EXP
Training Class	TRC
On the Job Training	OJT
Observation	OBS
Test	TST
Education	EDU

Evaluator

Clifton Aldridge	CA
[Name]	Initials
[Name]	Initials
Mark Northrup	MRN
Chris Hoover	CH
Instructor	INS

Color Key

Pending Skill Training
Completed Skill Training
LATE Skill Training

lote Instruction-related review / training
ncludes the related
STI = Instructions
STC = Checklists

Process	JR Lucero Device Engineer Planned	Eval. Method	Evaluator	Completed	Rachel Device Planned	Eval. Method
STP-001, Testing Process	11/30/11	OJT	CA	11/30/11	8/2/11	TRC
STI-001, SEM Examination	11/30/11	OJT	CA	11/30/11	1/30/12	TRC
STI-002, Internal Examination	11/30/11	OJT	CA	11/30/11	8/2/11	TRC
STI-013, Olympus BX50 Leica MZ80 - Infinity amera Operating Procedure	11/30/11	OJT	CA	1/24/12	8/2/11	TRC
STI-004, Wire Bond and Die Shear Test nstructions	11/30/11	OJT	CA	11/30/11	8/2/11	TRC
STI-012, Wet Saw Operation	11/30/11	OJT	CA	1/20/12	8/2/11	TRC
STI-014, Chemical Decapulation Instructions	11/30/11	OJT	CA	11/30/11	8/2/11	TRC
STI-015, Sample Mounting Instructions	1/24/12	OJT	CA	1/24/12	8/2/11	TRC
STI-016, Solderability Testing	1/24/12	OJT	CA	1/24/12	6/15/12	TRC
STI-005, XRF	1/24/12	EXP	CA	1/24/12	3/15/12	TRC
STI-006, Radiographic / X-ray Examination	1/24/12	EXP	CA	1/24/12	8/2/11	TRC
STI-007, PIND	11/30/11	OJT	CA	11/30/11	8/2/11	TRC
STI-008, Acoustic Microscopy	11/30/11	OJT	CA	11/30/11	8/2/11	TRC
STI-009, Seal Test Operation	1/24/12	OJT	CA	1/24/12	8/2/11	TRC

Dynamic Research and Testing Laboratories – Business Instruction

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL

	Document Title: **Pin to Pin Curve Trace**
	Document Number: **TSTI-043, Rev C**
Document Owner: **Jimmy Lucero** ***Backup Owner:*** **Clifton Aldridge**	***Approver(s):*** **Clifton Aldridge**
Parent Document: **TSTP-001, Testing Process**	***Notify of Changes:*** **All Dynamic Research and Testing Laboratories Employees**
Referenced Document(s): **JDI Analog and Digital Tester manual; TSTC- 054 Pin to Pin Curve Trace Spreadsheet, TSTC-055 Pin to Pin Checklist; SPOC 419 (Part Authenticity Testing – Statement of Work); MIL-STD-750 Method 4023, MIL-STD-883 Method 5003**	

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

DRTL and IEC Electronics

Certifications:

AS9100 / ISO/IEC 17025 / AS6171

ESD 20.20
BUREAU VERITAS Certification

Albuquerque, NM

Nadcap Accredited
Electronics

IPC 600/610/620/7711

IPC J-STD-001

ITAR

Memberships:

erai MEMBER

SMTA Surface Mount Technology Association

PROUD AIA MEMBER

SAE Aerospace G19 Counterfeit Electronic Components Committee

iNEMI

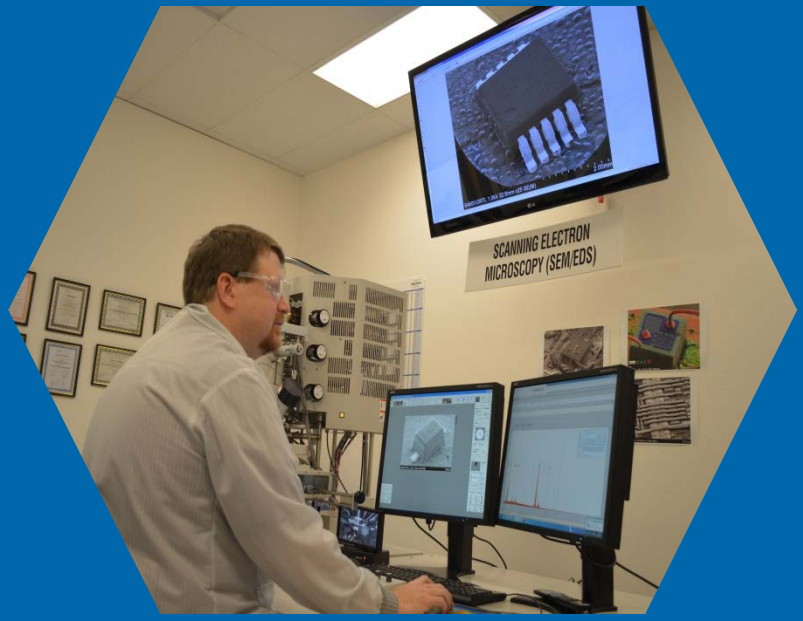
SAE International

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

DRTL Capabilities

Dynamic Research and Testing Laboratories (DRTL)

- Component Risk Mitigation
- Destructive Physical Analysis
- Failure Analysis
- Parts Screening
- Product Qualifications
- Material Qualifications
- Consulting Services
- ISO 17025 Certified



Our staff offers highly respected technical expertise, personable service, and quick response.

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC
DRTL
A Member of the IEC Electronics Family of Companies

Can You Afford Not To have A Risk Mitigation Strategy ?

Thank you !

DYNAMIC RESEARCH AND TESTING LABORATORIES, LLC

DRTL

A Member of the IEC Electronics Family of Companies